**Institute of Engineering & Management**

**Department of Computer Science & Engineering**

**Computer Architecture Laboratory for 2nd year 4th semester 2018**

**Code: CS 493**

**Date:** 17/02/18

**WEEK-2**

**Assignment-1:** Implementation of AND, OR, NOT, XOR, NAND, NOR gates using Xilinx ISE.

**Objective:** To implement OR gate

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device Family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top level source style | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **INPUT** | | **OUTPUT** |
| **A** | **B** | **Y** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Behavioral Model:**

**Data flow Model:**

**Code:**

**1. Behavioral Model Code:**

entity orgate is: port( a: in std\_logic;  
 b: in std\_logic;   
 c: out std\_logic);  
 end orgate;   
architectural behaviour of orgate is:   
begin Process(a,b)   
begin   
 if(a=’0’ and b=’0’)  
 then c<=’0’;  
 else c<=’1’;   
end if;  
 end process;  
 end behavioral;

**2. Data flow Model Code:**

entity orgate is:   
port( a: in std\_logic;   
 b: in std\_logic;   
 c: out std\_logic);   
end orgate;  
 architectural Dataflow of orgate is:   
begin   
c<=a or b;   
end Dataflow;

**Output:**

**Discussion:**